CHOOSING THE CORRECT CHIP SIZE PACKAGE FOR THE RIGHT APPLICATION

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ABSTRACT

With so many IC packaging options in today's electronics market, it has become difficult to discern between all the different packaging technologies. Often new packaging technologies are introduced to the market with certain performance levels. These levels of performance are compared via electrical, thermal, reliability, and density. Of course all of these characteristics have a certain cost base value to the customer-- Chip Size Package (CSP) type packages in particular.

It has been reported that CSP's will grow 6X by the year 2000, stated in CSP Markets and Applications. In fact, silicon suppliers indicate the growth of this market to likely exceed this prediction. It has been pointed out by many market analysts that despite the multitude of existing CSP's, the market will contain four types and they are known as the following: flexible interposer, rigid interposer, custom leadframe, and wafer scale. Each of these types of packages has its strengths and weaknesses.

This paper will describe the electrical, thermal, and reliability advantages of the rigid (PCB), flex (tape), and leadframe (copper) type CSP's that are offered in the market place (FBGA, TfBGA, LPCC). All are wirebond type packages that will gain most of the market share over flip chip type configurations to date.

INTRODUCTION

Now, more than ever the increasing demand for smaller, thinner, and lighter products are upon us. A few high density interconnect industry keywords such as: system-on-a-chip, lines & spaces, flex, laminate, package to die size ratio, miniaturization, lower inductance, rise time, burst speed, thermal impedance, shielding, socket, reliability, moisture level, z-height, re-distribution, and many other terms have resulted in a fighting packaging frenzy that could be called: "The War of Packages". All these terms are related to a package type that various market segments in the semiconductor industry are seeking. These include but are not limited to portable PC's, cellular, wireless, printers, routers, cameras, and cable to name a few. The high-performance, mixed-technology wireless communications and PC graphics systems ICs are the enabling technologies that drive demand for wafer-level interconnect designs. As many know to date the semiconductor industry is driven foremost by manufacturing cost, then features and performance. For the majority of the semiconductor manufacturers, it is still a wait-and-see attitude. Thus, "the ticket to paradise is still too high, and many are waiting to catch the next boat", as stated by the Semiconductors Worldwide Focus Report.

The "next boat" is here and a focused picture on how all these various package types will unfold is becoming bright. The drive towards smaller, thinner, and lighter end products has led to the phenomenal interest in existing Chip Scale (or Size) Packages for the portable electronic market. Table 1 outlines a variety of companies that offer various CSP configurations. As one analyzes the list of package types, it is obvious that four technologies exist on three preferred IC supporting platforms: Laminate, Flex, and Leadframe. Ceramic is acknowledged as well but due to proliferation of the below mainstream products and cost acceptance, ceramic will not be addressed.

Table 1. CSP Technologies Offered

Category	Type	Company
Flex Circuit Interposer	Tab/Flip Chip	GE,IZM, KME, NEC, Mitsubishi, Sony, ROHM, Tessera/ licensees
	Wirebonding	ASAT, Fujitsu, Amkor/Anam, TI, Hitachi, Sharp, Toshiba, LSI Logic
Rigid Substrate	Flip Chip	Citizen, Fujitsu, Matsushita, Sony, Motorola, Oki
	Wirebonding	ASAT, ASE, Amkor/Anam Fujitsu, Motorola, NEC, Rohm, Sony, Toshiba
Leadframe	Wirebonding	ASAT, Amkor/Anam,TI Fujitsu, Hitachi, LG, Samsung, Matsushita, Shinko, Toshiba, Dai Nippon
Wafer Level		ChipScale, Fujitsu, Tessera, EPIC, FCT, NEC, Sandia 3-D Plus, ShellCase

Source: TechSearch International Inc.

MAINSTREAM CSP PACKAGES

Rigid Substrate

The Fine Pitch BGA (FBGA) is similar to the PBGA in that it uses a Bismalimide Triazine (BT) or alternative laminate structure. The base laminate is limited to a current thickness of 0.25mm and is being produced in mass production.

The high-density substrate is manufactured in a panel format that has individual "pods", configured in an array format. The strip is introduced into the standard PBGA manufacturing line in which die attach, wirebond, and overmold are performed. The large mold body will cover a multiple of array products that are then marked, bumped, and singulated. The singulated process is what makes this near chip scale package unique (Package:Die Size = 1.33). Figure 1 shows a cross section of the laminate FBGA structure.

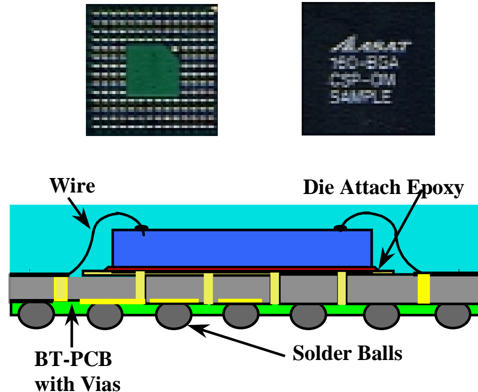

Figure 1. Fine Pitch BGA Package Cross-section.

Dicing. The process uses conventional dicing saw techniques where the processed strip is mounted with the solderballs upward onto a carrier ring, aligned, and sawed. The singulated strips in carrier rings are then transferred to a high-speed pick-and-place machine and the units are placed into a JEDEC tray for test. Therefore, let it be noted that this operation methodology will not only apply to laminate but also to polyimide tape and leadframe based near CSP package type constructions, outlined in this paper.

The results from the automatic wafer saw alignment systems have been very encouraging to date. But, the process is obviously capacity limited and costly. Process optimization is continuing to reach higher cutting speeds by using thicker tape and define blade parameters for specific packages; but it is still the bottleneck to meet today's demand. For initial process start-up and certain volume levels the current process equipment and methodology is fine. As the process throughputs, gated by sawing feed rates, increase it is realized that multiple-blade gang sawing along with loading is needed. The equipment suppliers are addressing these needs but not as fast as the demand for these products. Until then, the value added of multiple units in an over-molded matrix array format will be gained.

Design. The design configuration using this near CSP package construction allows the customer to gain product acceptance to the market quickly at a relatively low cost. The materials are well established, qualified, and known. The only difference is processing multiple packages in a matrix format and saw singulated. The majority of the packages uses standard design rules of 0.060 - 0.100mm lines and spaces with 0.2-0.3mm vias. The pad pitch used is a comfortable 0.8mm and can be provided in a full or peripheral array format to meet motherboard cost and routing demands. The 0.5mm pitch can be achieved but unique concentric squares must be featured to achieve routability. This is obviously a limitation, if motherboards cannot route to a full 0.5mm pitch array. This is where one would utilize the film circuit base substrate to achieve the higher density needed.

Film Circuit

The film base substrate is typically composed of a polyimide like dielectric material with one or more layers of patterned circuitry. The one metal pattern circuitry is Electro-deposited (ED) copper covered with nickel and gold for bondability and solderbility. The ED copper is typically laminated onto the film prior to typical TAB processing techniques. It is well known that the notable features of the flexible circuit film are its thinness, high circuitry density, and electrical performance. The most common known chip size packages, using a flex-based interposer, are µBGA (micro Ball Grid Array) and FxBGA (Flex Fine Pitch Ball Grid Array).

µBGA™. The µBGA is unique in construction and has been mainly geared towards memory applications. It uses a flexible circuit film as the substrate material. The die is attached to this material with a low stress, elastomeric adhesive. The circuit traces on the tape are formed into leads and these leads are bonded directly to the bond pads on the chip. The elastomeric encapsulant surrounds the leads and chip bond pads. The solder balls are then attached to ball pad openings on the tape and then singulated. The encapsulant material is noted to extend a distance beyond the edge of the chip 0.2 - 0.4mm. The construction is noted in Figure 2.

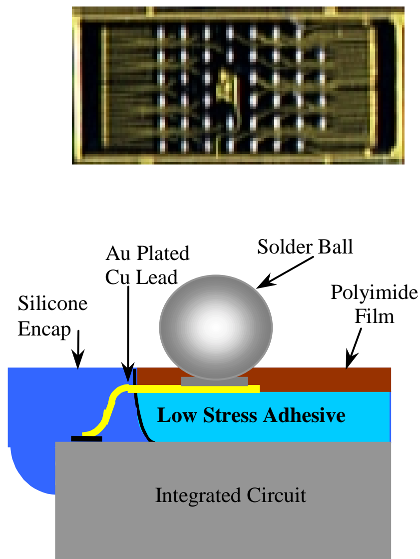

Figure 2. µBGA Package Construction
Note: The µBGA™ is a Trademark by *Tessera*

The µBGA, by definition, is a chip scale package. The package is typically die size + 0.5mm which meets the true definition of a CSP (Package:die = 1.2). The package thickness is known to be less than 0.9mm.

It is well known that the low stress die-attach adhesive/elastomer decouples the CTE mismatch of the chip from the circuit film and solderballs. This allows excellent solder joint reliability of the surface mounted package. Published data has shown this package to exceed 1000 cycles of thermal cycling from 0 - 100C. Of course this is dependent on package size, die size, solder ball size, test board thickness and finish. Also, soldermask defined or non-defined as well as opening dimensions can contribute to solder joint fatigue life.

FxBGA. The flex Fine Pitch BGA takes advantage of the high routability, lines and spaces, and z-height that (BT) laminate cannot deliver. The construction contains a polyimide film based substrate where holes are punched, etched, and/or laser drilled prior to ED copper lamination. Figure 3 shows the FxBGA manufacturing process-flow using the punching method. The holes allow the solderballs to contact the single metal layer tape from the bottom where the circuitry is etched to the topside capture pad. Figure 4 shows a cross-sectional view of this package construction.

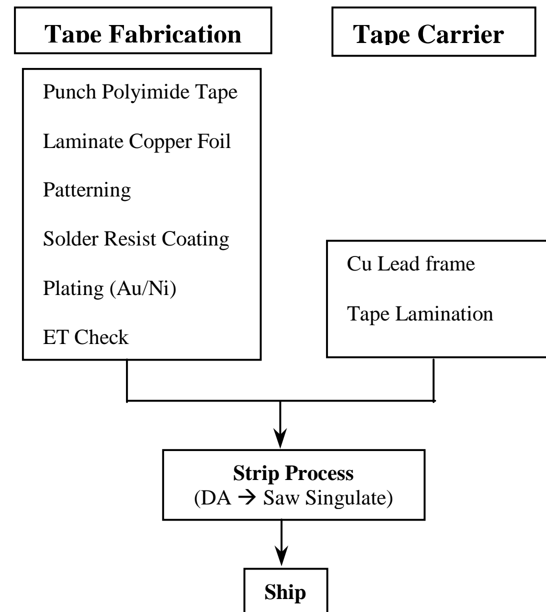

Figure 3. FxBGA Tape Process Flow

The FxBGA is not limited to a one metal layer construction, but two metal layers between the polyimide dielectric can be used as well. The metals are either laminated or evaporated to provide a higher density circuit. The same design rules can be used on single metal tape, and it would not affect the choice of structure. Thus, the only difference will be in the cost of tape (two layers versus one).

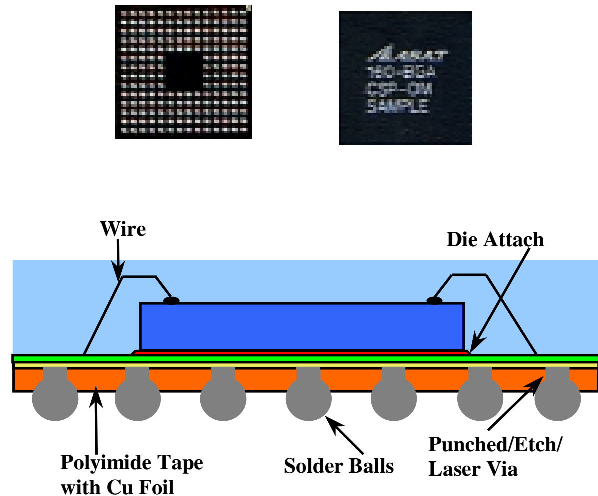

Figure 4. Cross-section view of the FxBGA.

The finished product received from the tape supplier is then laminated on a metal frame to hold the flex tape in place for standard wirebond (or flip chip) assembly type processing (Figure 3). The FxBGA, mentioned earlier, is of the saw singulated type as shown in Figure 4. Some key features of the FxBGA are given below:

- Full routable perimeter and full matrix arrays.
- < 1.0 mm package z-height when mounted.
- Increased routing density capability over laminate near chip scale packages.
- Ball-pitch of 0.5mm in x- and y- directions
- Improved electrical parasitics

Metal Lead-frame

The metal lead-frame near chip scale package is a CSP solution created to address the market need for cost, substrate lead-time, and replacing conventional leaded and single small outline packages (SSOP). This package, known as the Lead-less Package Chip Carrier (LPCC), is approximately half the size of conventional packages and mounted height is <0.9mm. The package is manufactured similar to the FBGA, and the FxBGA where a matrix configuration on an etched leadframe is used. The etched lead-frame is die attached, wirebonded, and over-molded. The transfer molding process utilizes standard BGA type processing techniques allowing a metal paddle to be exposed. The strip is then introduced to a de-flashing process to remove the excess mold compound around the leads and exposed paddle prior to tin-lead plating. Let it be noted that a surface finish of Nickel-Palladium can also be provided. The lead-frame is then saw-singulated using similar process techniques as described above for the FPBGA and FxBGA. Figure 5 represents a cross-sectional and backside view of this package type.

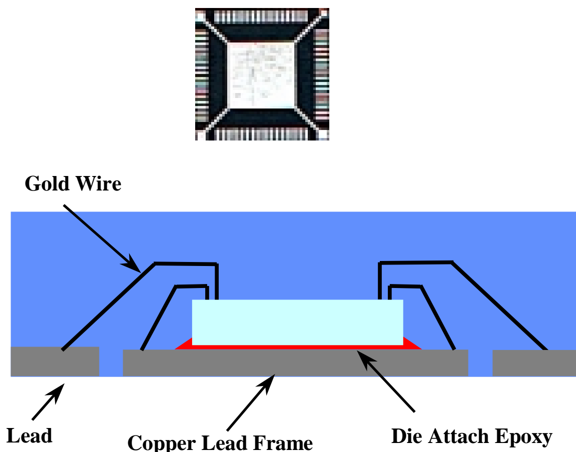

Figure 5. The LPCC Package side and bottom view.

This family of packages provides the designer the advantages of reliability level and ease of attachment of the SSOP. The LPCC construction allows homogeneous electrical parasitics as well as improved thermal resistance over conventional packages. The open tooled lead-frame allows non-specific net-lists to be maintained and provides multiple customers to gain access to lead-frame designs that are universal in nature. In turn this drives volume and improves the cost base of the package. Some key features of the LPCC are outlined below:

- Uses a combination of tooling from standard and FBGA packages
- High Flexibility for new designs
- Design lead times including leadframe, 10 days
- Ease for mother board routing
- Extended die paddle can be used for ground plane bonding.
- Exposed die paddle for improved thermal path as well as solder joint stress.
- Small foot print
- Mounted height <0.9mm
- Controlled mutual inductance
- Can be offered with solder balls

The product is well suited for I/O's less than 100. Particular for body sizes of 4x4mm - 6x6mm where substrate and tape costs are limited when a few I/O's are required.

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PERFORMANCE

Electrical & Thermal

Electrical. Electrical criteria are becoming more prevalent as device speeds and power requirements increase. There was a time when any parasitic effect from the package was insignificant because the package size to device performance was small enough to be of minimal consequence.

Today’s devices have changed that philosophy. For high performance devices of today, the package has become the major inhibitor. By analyzing the package, an engineer can use both measurement and modeling tools to identify the electrical parasitic parameters. Once the parasitics are quantified, descriptive interconnect models can then be created and added to the circuit I/O drivers to represent the interaction of the device and the package. A simulation can be performed at the circuit level to understand the effects of the parasitics on the device performance. Post processing includes evaluating parameters such as noise (coupling, switching, ground bound), signal integrity, timing, delay, and, at the board level, electromagnetic interference (EMI). From there, the engineer can make the necessary decisions on how to improve the existing package design, construction or material, or change to another type of package to achieve optimal performance.

The electrical parasitics of the 9x9mm LPCC, 12x12mm FBGA, and 12x12mm FxBGA were modeled using an EM Solver IE3D and displayed graphically in Figure 6. The spread in self-inductance among each package is due to trace length variation between the

longest trace and shortest trace which includes 1.0 - 1.5mm wire length (33 micron wire diameter) and the solder ball. The variation of inductance between FxBGA and FBGA than the LPCC is due to the consistency of lead and wire lengths throughout the package. The mutual inductance between neighboring leads is lower on the FxBGA due to the fact that the dielectric constant is low (3.5) compared to BT (4.3). The mutual inductance on the LPCC is higher since there exists minimal dielectric of mold compound between the lead, when comparing this structure to FxBGA and FBGA. Although there are minor variations in parasitics that exist in all three packages, it is quite evident that materials, design layout, and mechanical configuration result in the degree of performance.

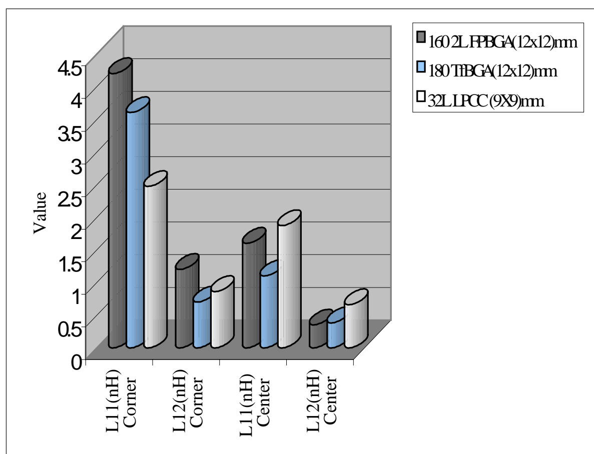

Figure 6. Mutual and Self Inductance for the FBGA, FxBGA, and LPCC

Thermal. As semiconductor companies have continued to reduce the IC size and add more functionality at higher speed, the power generated by the IC continues to increase. Therefore, the design and materials used in the electronic package play an important role in providing a thermal path from the IC to ambient. As the primary interface, the package can be a major influence on the IC performance. By characterizing the package to determine its thermal resistance an engineer can understand the effectiveness of the packages' thermal dissipation through the existing path of the device, allowing a cost-performance analysis to be performed as part of the package selection process.

For this case, thermal modeling was performed to understand the junction-to-ambient thermal resistance (θja) using a commercially available Finite Element Analysis (FEA) software (ANSYS). The thermal analysis for the package characteristics was conducted on the various near-chip scale packages discussed and represented in Figure 7. The model consisted of a 4.0x4.5x0.062 inch 2S0P-test board at zero airflow. The power dissipation used was 1 watt and a die size of 5x5mm so consistency in the model for all packages measured could be observed.

It was found that the LPCC had the lowest thermal resistance, between the packages measured, due to the die mounted directly on to a metal frame and the backside pad mounted to the PCB. Hence, allowing the majority of the heat to dissipate rapidly into the PCB. The film-based showed a significant improvement over the laminate-based product due to the thinner substrate material and the solder balls directly contacted to the die paddle and wire bond pads. The heat generated within the FBGA package is greater of the three packages. This is due to the heat trying primarily being expelled through the solder balls and into the thicker substrate, (laminate), where it will spread through the board and dissipate into the ambient. One of the potential thermal bottlenecks is the heat flow from the die through the substrate and molding compound to the solder balls as indicated in the data. The closer position and distance the balls are to the die the less thermal resistance will result, in return an improvement in the thermal performance.

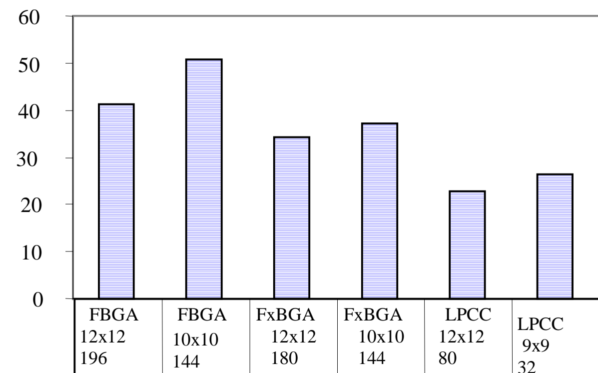

Figure 7. θja Thermal Resistance (°C/W) of the FBGA, TfBGA and LPCC for various body sizes.

Reliability

Environmental. The FBGA have passed internal and external reliability qualification. A summary of typical reliability tests performed is listed in Table 2.

Table 2. FBGA Package Level Reliability Passed

Test	Condition
MSL 3	30C/60%RH/ 192 Hrs.
MSL 2	85C/60%RH/168 Hrs.
MSL 1	85C/85%RH/168 Hrs.
Autoclave	121C/P=15psig/100%RH/168hrs
Temperature Cycle	-65C<=>150C 500/1000Cycles
Thermal Shock	-65C<=>150C 250/500 Cycles
HAST	130C/85%RH/96 Hrs.
HTSL	150C/1000 Hrs.

*Note: MSL testing was conducted using a 4 zone IR Reflow oven with a maximum reflow temperature of 225C.

The initial reliability for the FxBGA and the LPCC looks promising. Internal data has shown that the product can meet a minimum JEDEC moisture sensitivity level of 3 and a minimum reliability equal to the data outlined in Table 3.

Table 3. Reliability Data Passed for FxBGA and LPCC

Test	Condition
MSL 3	30C/60%RH/ 192 Hrs.
Autoclave	121C/P=15psig/100%RH/168hrs
Temperature Cycle	-65C<=>150C 500 Cycles
Thermal Shock	-65C<=>150C 300 Cycles
HAST	130C/85%RH/96 Hrs.
HTSL	150C/1000 Hrs.

*Note: MSL testing was conducted using a 4 zone IR Reflow oven with a maximum reflow temperature of 225C.

Typical failures found for FBGA, FxBGA, and LPCC has shown to vary in delamination locations. The FBGA (BT laminate) has shown to delaminate around the bond fingers at levels 2 or 1. The FxBGA (polyimide flex) tends to delaminate primarily under the die region. The focuses to move towards an alternative die attach material for polyimide material type structures is imperative for this package configuration. Non-conductive and conductive die attach material types are currently under qualification to assure a robust structure, above moisture sensitivity level 3. The LPCC, lead-frame CSP, initially has shown to be the most robust structure under moisture sensitivity level testing. This is a function of package size as well as die size. Tests conducted to date have been on 4x4mm and 9x9mm structures. The consistent success of moisture level testing has been due to the fact that the backside of the die paddle is exposed. This minimizes a prone interface of failure that occurs between the mold compound and lead-frame that exists in standard packages.

Board Level Testing. The key to the success of these near chip and chip scale packages is additional board level reliability. With the decrease in pad geometry's as well as the solder ball size lower standoff heights are achieved. The result, is a reduction in cycles to failure at the motherboard level compared to standard BGA packages that use 1.27mm type pitches. The industry goal is to achieve a minimum of 1000 cycles of air to air Temperature Cycle (TC) from -40C ⇔ 125C. The packages presented --FBGA, FxBGA, and LPCC-- has demonstrated this to be the case through actual test measurements or modeling at external and internal test sites. The primary variables for each package that achieved 1000 cycles of TC testing are presented in Table 4.

Table 4. Near CSP Package Design Variables

Package	Size	Ball Size	Pitch	Pad Size	Die Size	Pad
FBGA	12x12	0.4	0.8	0.4	7x7	SMD
FxBGA	12x12	0.4	0.8	0.35	7x7	Punch
LPCC	9x9	-	0.5	0.25x0.4	3x3	Sn:Pb

Note: All dimensions are in millimeters

All the test boards used were FR-4 type with a non-soldermask defined pad measured at 0.35mm. Test boards and data was gathered by and reported verbally from the customer. A follow-up on test set-up and test board configuration is necessary to understand the failure and limits of the data. Published data by Mawer supports the FBGA and FxBGA findings of 1000 Cycles from the customer.

Package Price

As reliability and design standards evolve, the CSP package will become more accepted in the market and the end users will provide more design wins for these package configurations. In return the volume will increase and the current price per ball will decrease. Today the packages being offered are relatively new in technology, resulting in higher variable and fixed costs. Advancing efficiencies in the assembly process, materials, equipment, and design standards will drive down prices. It has been reported by ETP Inc. that the over all average CSP price per I/O is expected to drop 60% from 1997 to 2002 (0.014 - 0.0085 USD/ball). Depending on the technology in materials and process as well as product stability to reach certain volume levels the price per ball could fall below 0.0085. The initial introduction to the LPCC package has shown to be cost effective in the low I/O counts (16-32) compared to FBGA and FxBGA. Initial high volume price/lead have fallen below 0.007 USD/lead.

CONCLUSION

The near CSP and CSP packages cover a wide range of ball, lead-count, and body sizes that are being offered in the market today in rigid, film, or metal base form. The characteristics of the FBGA, µBGA™ FxBGA, and LPCC packages have been described. The mainstream packages are wirebonded using a dice and saw technique in a matrix strip format. The matrix format is used to maximize material utilization and improve process efficiencies to obtain an optimal cost/ball at high volume. The electrical and thermal performance has shown to improve as routing density increases and substrate thickness decreases. The material type of the substrate used has shown to improve the electrical and thermal performance as well.

All near size CSP packages discussed has shown to pass a favorable JEDEC Level 3 preconditioning along with post reliability testing. Customers board level testing has resulted in the packages to pass a minimum of 1000 cycles of -40C ⇔125C air-to-air Temperature Cycle. This is consistent with published data in the field. Continuous process improvement in materials and design will contribute to increased quality of the package. If no overriding requirement necessitates choice of particluar package, it is advisable to select a type incorporating proven technologies with the longest history of reliability. Further, as the price and performance of these packages improve the opportunity of market size will continue to increase at or beyond the predicted levels reported.

Note: The µBGA™ is a Trademark by *Tessera*

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