COST/PERFORMANCE ANALYSIS OF HIGH PIN COUNT SURFACE MOUNT PLASTIC PACKAGES

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ABSTRACT

Surface mount packages come in various forms, most of which are industry standards. Increasing demands on electronic packaging by the semiconductor industry has led to recent developments in plastic surface mount package technology. These packages are finding applications in areas such as PCMCIA and portable products, as well as the standard desktop computer products. There is even a growing interest in plastic packaging in the defense and microwave electronics industry. Such packages include quad flat pack (QFP) type packages, both with and without internal heat slugs or heat spreaders, ball grid arrays (BGA) and thermally enhanced ball grid arrays.

One of the most important industry drivers today is packaging cost. Cost can be related to a number of variables: package materials, assembly, yield, test, reliability, board yield, and performance. In comparison to earlier surface mount packages, these packages provide many improvements on these variables, yet none have proven to be perfect in all categories. In fact, the selection of the "optimal" package is usually application-specific. This paper will address the area of cost, as related to the electrical and thermal characteristics inherent to the packages and provide several figures of merit that will allow the end user to weigh the advantages of these packages under different application environments.

INTRODUCTION

Table 1 shows the types of packages characterized in this paper, which include: standard PQFP, PQFP with internal heat spreader, MQUAD™ QFP, PowerQuad™ QFP, Edquad™ QFP, standard PBGA, SuperBGA™, MBGA™, and the TBGA. The analysis will show both relative and comparative performance versus cost of the periphery and array types of packages that are available today. Since there are slight variations between the packages (body size, lead count, cavity size, wirebond length, heat spreader design and material), the results will not be absolute. Yet, figures of merit will be created, based on parameters measurable in the study.

To make a meaningful comparison, the packages will be measured and modeled under the same conditions, using JEDEC [1-3] standard procedures. The procedures will be cited and explained, and the exact conditions will be provided, so that the results can be duplicated.

DISCUSSION

Two areas determining "performance" of a package relate to its ability ensure the device(s) encased in the package is not restricted either thermally or electrically. Design, materials, and construction of the package determine the performance characteristics. Each parameter has its set of flexibility and limitations and some of these parameters overlap. In other words, some packages can be designed to have enhanced electrical performance, yet be restrictive on thermal performance, or vise versa.

Thermal issues have become an ever increasing inhibitor in device performance and contributor to cost. As semiconductor companies have continued to reduce the IC size and add more functionality at higher speed, the power generated by the IC continues to increase. Although voltage levels have slowly decreased, the amount of current needed to drive (or power) the IC has increased. Therefore, the design and materials used in the electronic package play an important role in providing a thermal path from the IC to the outside world. As the primary interface, the package can be a major influence on the IC performance, due to the presence or absence of the heat generated by the device. By characterizing the package to determine its thermal resistance at various junctions, an engineer can realize the effectiveness of the package as a thermal path for the device, which allows a cost-performance analysis to be performed as part of the package selection process.

Electrical issues are also becoming more prevalent as device speeds and power requirements increase. There was a time when any parasitic effect from the package was insignificant because the package size to device performance was small enough to be of minimal consequence. The system level interconnects were the major inhibitors due to physical size and interconnect density. Today's devices have changed that philosophy. For high performance devices of today, the package has become the major inhibitor. By analyzing the package, an engineer can use both measurement and modeling tools to identify the electrical parasitic parameters. Once the parasitics are quantified, descriptive interconnect models can then be created and added to the circuit I/O drivers to represent the interaction of the device and the package. A simulation can be performed at the circuit level to understand the effects of the parasitics on the device performance. Post processing includes evaluating parameters such as noise (coupling, switching, ground), signal integrity, timing, delay, and, at the board level, electromagnetic interference (EMI). From there, the engineer can make the necessary decisions as to how to improve the existing package design, construction or material, or change to another type of package to achieve optimal performance.

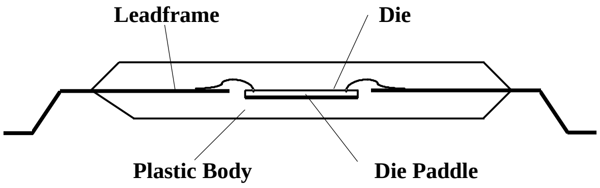
PACKAGE CONSTRUCTION

Plastic packages are available in several formats. The selection criteria should aim towards providing the necessary performance while maintaining an allowable cost. This paper will address only high lead count, high density packages. This is because the high I/O types of packages accommodate high density, high functionality integrated circuits, requiring higher thermal capacity and lower parasitics than low density packages. Competitive industry pressures also demand continual improvement in the cost to performance ratio for these higher pincount packages.

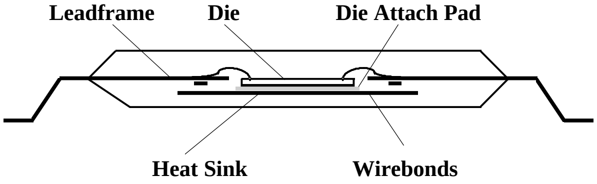
Plastic Quad Flat Pack Package

This package has been used in the industry for many years. JEDEC has standardized on the mechanical dimensions of this package, determining its overall body size, lead configuration, standoff, body thickness and lead counts. Internal to the package, the packaging designer is allowed to create a leadframe design which is restricted only by the leadframe manufacturer's etching or stamping ability or assembler's wirebonding capability.

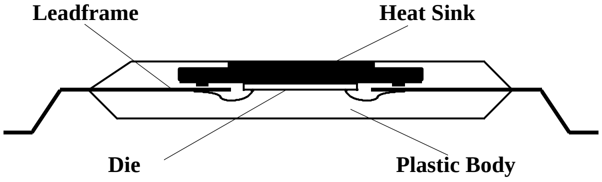
Thermally enhanced QFP's also maintain JEDEC standard dimensions. Yet, the internal construction may vary depending on the ultimate goal of the packaging designer. Figure 1 shows the cross-section of various QFP's, including the configurations with heatspreader. There are types with "drop-in", as well as exposed heat-slugs, with costs and performance considerations for both. The heatspreader can be physically designed to maximize process capabilities and cost as related to performance. Various drop-in configurations include: solid square or rectangle, starburst, union jack, or circular. The packages with exposed heatspreader designs include circular (Edquad™) and chamfered square (PowerQuad™) designs.



A) Standard Configuration



B) Drop-In Heat Spreader



C) Exposed Integrated Heat-Slug, Die-Down

Figure 1. Thermally Enhanced QFP Variations

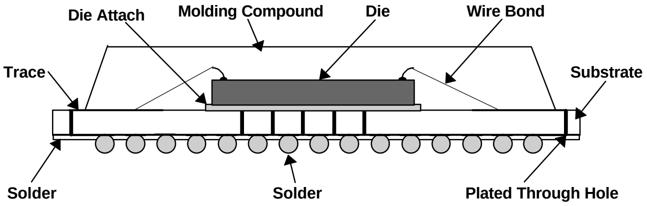


Figure 2. Plastic Ball Grid Array (PBGA)

Plastic Ball Grid Array (PBGA) Package

A cross-section of a typical PBGA is shown in Figure 2. The PBGA package design utilizes a single or multilayer, bismaleimide triazine (BT) or other resin-glass-cloth type substrate. The die is attached to the substrate with silver-filled epoxy, and gold wire bonds are used for die-to-substrate interconnects. The die is also encapsulated by either a transfer molding process using typical low-stress molding compound or a liquid dispensed epoxy based encapsulant material. The traces (conductors) are typically fanned-out from the bond fingers to the periphery of the substrate, fed through the board with plated through holes, and routed to the array of solder ball pads. Low melting point solder balls (63Sn37Pb) are attached to the substrate on these Ni-Au plated pads.

Cavity Plastic Ball Grid Array (CPBGA)

This package is designed to be a high-performance package with enhanced thermal and electrical design options. A cross-section of a typical construction is shown in Figure 3. Construction is of a laminate design, allowing the option of multiple layers and bonding tiers. The die is attached with silver-filled epoxy and gold wire is used for bonding the chip to the package. The cavity is filled with liquid encapsulant to protect the die and wire bonds. Low melting point (63Sn37Pb) solder balls are attached around the cavity to the substrate. Other references to this type of package are enhanced ball grid array (EBGA) and SuperBGA®[7].

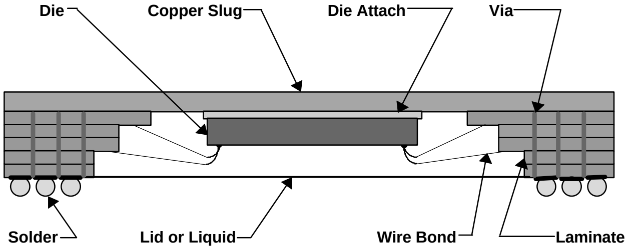


Figure 3. Cavity Plastic Ball Grid Array (CPBGA)

Tape Ball Grid Array (TBGA)

There are a number of configurations for the TBGA being developed in the industry today. The basic construction consists of a copper/polyimide flex tape to route from the interconnect mechanism on the die to the solder balls, and a copper heat spreader. The die attachment and interconnect mechanisms vary, depending on cost and application. So far, there is a flip chip, TAB, and wirebonded interconnect approach. Figure 4 shows a flip-chip version and Figure 5 shows a wirebonded interconnect approach.

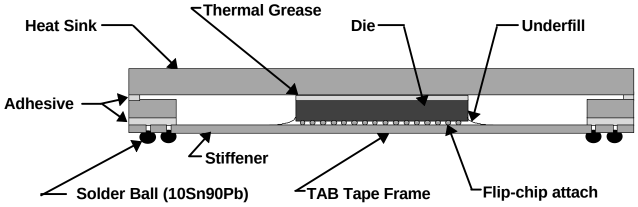


Figure 4. Flip-Chip Tape Ball Grid Array (TBGA)

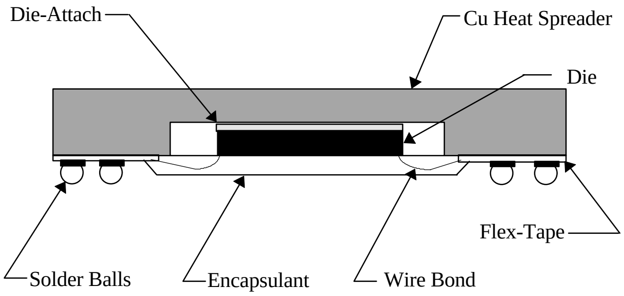


Figure 5. Wirebond Tape Ball Grid Array (TBGA)

THERMAL PERFORMANCE METRICS

Thermal performance of a given package is directly dependent on the environment of the system in which it is placed. Well known effects include temperature and air speed, or the addition of heat sinks external to the package. Other effects, such as mounting surface effective thermal conductivity, adjacent component contribution to thermal loading, and small enclosures that disallow the formation of free convecting cells, are not as well known or as fully characterized.

The idea of a single thermal resistance describing the thermal performance of a package is not valid, therefore data supporting a precise description of the environment in which it was measured is a requirement. Recently, the EIA/JEDEC JC15.1 subcommittee has published several specifications dealing directly with this problem (thermal refs to JC15.1 specifications). Using these standards as references, repeatability is improved and information for system designers is more realistic and usable.

All thermal data reported herein was generated using the EIA/JEDEC JESD51 standards series, thus additional information in the text related to reporting requirements is present. This method allows consistent comparison of the various packages investigated in this paper.

Table 2. Thermal Resistance Measurements

Package Type on 4-Layer PCB	θ_{JA}, ^{o}C/W Air Speed, lfpm					θ_{JC}, ^{o}C/W
	0	100	200	400	600	
208 QFP	26.8	24.4	23.3	21.6	19.4	7.0
208 QFP-TEP	17.6	15.1	14.0	12.6	10.8	4.7
208 MQuad	16.9					
208 PQuad	13.3	9.4	7.9	6.5	6.0	0.5
256 PBGA	30.5	25.4	24.7	23.5	20.7	N/A
256 MBGA	12.8	9.3	8.4	7.8	7.3	0.6
256 SBGA	14.1	11.1	10.1	9.4	9.0	0.35
240 PQuad	11.5	6.8	5.5	4.6	4.0	1.8
352 SBGA	11.6	7.3	6.3	5.8	5.4	0.34

The thermal data in Table 2 was measured using standardized test boards of a four layer design (2S2P). The environment was a box constructed of low emissivity chamber with a one cubic foot volume. Power dissipation for the tests was on the order of 1.2 to 2.0 watts.

For comparison of different package styles, all geometric, electrical, and mechanical environments must be taken into account. As can be seen from the data, the die size (see Table 1) varies from 0.298" x 0.294" to 0.458" x 0.458". Die area will affect thermal resistance results mildly in the traditional PQFPs, drop-in heat sink PQFPs and in PBGAs, but the change is more pronounced in heat slug PQFPs and TBGA's. In the former cases (PQFP, PBGA) the die paddle size is much more closely coupled to the thermal resistance, showing a significant decrease in thermal resistance for larger die paddle sizes. In the latter case (heat slug PQFP, TBGA) the die size comes into play. For example, changing the die size on a heat-slug PQFP from 300 mil^2 to 445 mil^2 causes only an approximate 6% decrease in thermal resistance. Due to the small variations in die size for the packages evaluated in this study, the comparisons are considered valid and should serve as a reasonable guide to the design tradeoffs.

ELECTRICAL PERFORMANCE METRICS

Electrical performance of high density packages is another fundamental concern. For many applications, the electrical characteristics of the package can be described by the lumped element inductance (L), capacitance (C), and resistance (R) of the interconnects. These parameters are dependent on frequency, proximity of package conductors to ground planes and to each other, and on material properties. Other electrical performance attributes associated with a package include time delay (t_d) and characteristic impedance (Z_0).

L, C, and R values are typically measured or modeled for a fixed frequency range or at the typical frequency that the device is expected to operate at. Although all packages have these properties, they are, for the most part, unwanted and can only limit system performance.

Inductance is most problematic for power supply interconnects, as power or ground noise is generated by the combination of simultaneous switching output currents and the interconnect inductance (Ldi/dt effects). If the magnitude of this noise is above the allowable device thresholds, non-switching or false switching can occur.

Capacitance can introduce problems if either characteristic impedance or timing delays are of a concern. Excess capacitance on the signal lines can create delays, but typically are not problematic if the interconnect length is short, as in the case of packaging. Power and ground capacitance can be built into packages with multiple layers (substrate) or with heatspreader or heat slugs (leadframe), and can actually act as decoupling mechanisms for simultaneous switching noise.

Most of the materials used for these high density packages use a low resistance metalized material for the leadframe or traces, typically copper. This property usually has the least impact on the signal integrity. Only at high frequency is this parameter of concern due to skin effects.

Package parasitics are measured using JEDEC guideline EIA/JEP 123, which include techniques involving time-domain reflectometry (TDR), impedance analysis (LCZ), and or vector network analysis (VNA) equipment and calibration. Each of the three techniques has its own merits, based on accuracy, ease of use, cost, fixturing, and frequency range. The measurement environment includes a ground plane which is located directly beneath the package leads/balls. Only 50% of the leads are connected to the ground reference, and are located opposite of the lead-under-test. The purpose of the 50% grounding is to give a “worst case” analysis of the package parasitics. This is not representative of a real configuration, but is both repeatable and easily set up for modeling.

COST/PERFORMANCE ANALYSIS

As mentioned in the beginning, cost and performance can be determined in many facets. The cost listed in Table 3 shows the relationship between various packages in size, I/O density, cost per pin, and total cost of the package. This cost includes the package, assembly, overhead and labor. It is important to note that cost is **NOT** related to price. There cannot be an association be cost and price, simply because one is based on fixed manufacturing cost and the other is based on what the market is willing to pay. Therefore, it is in no way assumed that any one of the packages analyzed are sold at a higher or lower price that the cost presented in this paper.

However, understanding cost can help understand the benefits of one package type versus another. For example, there may be multiple sources for one type of product, such as the generic PQFP package, and a window of price offerings for the package. But generally, the cost of the package is fundamentally similar. It will vary slightly by such factors as volume of materials used, automation of assembly, overhead and labor cost associated with facility assembly location and sophistication.

The numbers derived for this study comes from various sources and cost analysis techniques. The relationship of cost to the performance criteria discussed previously is shown in Table 3. As can be seen in the table, and in Graph 1, there is a figure of merit (FOM) given to the packages analyzed, based on the following formula:

$$FOM = \frac{\text{I / O density}}{\text{Cost density} \bullet \Theta\text{ja } d\text{ensity} \bullet l \text{ density}}$$

where the I/O density is calculated from the lead count to body size in I/O/mm^2, Θja density is the thermal resistance density in ^{o}C/W/mm^2, λ density is the parasitic inductance density in L/mm2, and the Cd is the cost density in $\$/\text{mm}^2$.

The analysis shows a cost/performance advantage of the thermally enhanced packages over the standard plastic packages. It also indicates the BGA packages have a better figure of merit over the QFP types. This can be significant when using performance as a determining factor for package choice.

Table 3. I/O Density & Cost

Ref	I/ODensity	Cost	Total Cost
#	(/mm2)	(¢/pin)	($/pkg.)
1	7.4	1.07	2.23
2	7.4	2.09	4.35
3	7.4	2.38	4.95
4	7.4	2.65	5.51
5	7.4	2.78	5.78
6	7.5	1.07	2.57
7	7.5	2.47	5.93
8	7.5	2.65	6.36
9	7.5	2.74	6.58
10	9.5	3.09	7.91
11	9.5	3.45	8.83
12	9.5	3.42	8.76
13	9.5	2.89	7.40
14	10.1	3.11	10.95
15	10.1	3.51	12.36
16	10.1	3.49	12.29
17	10.1	2.95	10.38

SUMMARY

A number of high pin count surface mount plastic packages were analyzed using standard methods and procedures to determine their electrical and thermal performance. A figure of merit was given to those parameters based on the relationship between the characteristics, I/O density and cost. A graph was created to highlight the significance of cost/performance of these types of packages, and can be used as a reference when considering a package of this type. As the cost of these packages are reduced, the associated Figure of Merit will increase, thus realizing the potential future advantage of these packages in high performance applications.

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Table1. Package Configuration Table

Key	Package Type	Body (square)	Cavity/ Die	Substrate or LF	P-D (watts)	Comments
1	208 PQFP	28 mm	Up	LF	2.0	measured 4L board
2	208 PQFP Drop In	28 mm	Up	LF	3.1	measured 4L board
3	208 PQFP MQuad	28 mm	Down	LF	3.3	measured 4L board
4	208 PQFP PowerQuad	28 mm	Down	LF	4.1	measured 4L board
5	208 PQFP Edquad	28 mm	Down	LF	3.3	measured 2L board
6	240 PQFP	32 mm	Up	LF	2.1	measured 2L board
7	240 PQFP MQuad	32 mm	Down	LF	3.5	modeled 4L board
8	240 PQFP PowerQuad	32 mm	Down	LF	4.8	measured 4L board
9	240 PQFP Edquad	32 mm	Down	LF	3.4	measured 2L board
10	256 PBGA	27 mm	Up	Substrate	1.8	measured 2L board
11	256 MBGA	27 mm	Down	Substrate	4.4	measured 4L board
12	256 SBGA	27 mm	Down	Substrate	3.9	measured 4L board
13	256 TBGA	27 mm	Down	Substrate	5.5	modeled 4L board
14	352 PBGA	35 mm	Up	Substrate	3.1	modeled 4L board
15	352 MBGA	35 mm	Down	Substrate	5.5	modeled 4L board
16	352 SBGA	35 mm	Down	Substrate	4.7	measured 4L board
17	352 TBGA	35 mm	Down	Substrate	7.1	modeled 4 layer

Graph 1.