

SIP

System-in-Package

With its core competencies in advanced package design, assembly and testing, ASAT is qualified to meet the electronics industry's demand for higher levels of integration, cost effectiveness and better electrical performance.

Using state-of-the-art design tools and electrical simulation, single or multiple chips, passive components and discrete devices can be designed into a standard or custom package. These elements can be electrically interconnected to the substrate in both chip form (wire bond or flip chip options available) and pre-tested assembled monolithic packages. Various leaded, and array package formats are supported.

Advantages

- Electrical performance improvement
- Real estate savings on printed board
- Shorter electrical paths
- System integration through high packaging density
- Faster time to market

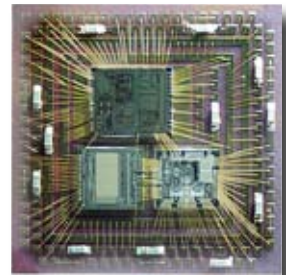
Typical Applications

- High-performance network interface
- Motion sensors
- Imaging applications
- Multimedia cards
- Handheld electronics
- RF applications
- Automatic test equipment

Features

- Leaded, array and leadless form factors
- Die only, tested packages and component configurations
- Laminate (plated through hole and build-up) ceramic, lead frame substrates and TAPP technology
- Flip chip, wire bond, silicon on silicon, and stacked assembly options
- EIA 0201 and 0402 passives

SiPs are constructed with standard materials and can be designed to meet your special packaging requirements.



SiP

Standard Materials

Solder Paste	Conventional and Pb-free
Die Attach	Conductive/Non-conductive
Discrete Attach	Solder and Conductive Epoxy
Gold Wire Diameter	1.0, 1.2 and 1.3 mils
Mold Compound	KMC-XXX and EME-XXXX Series
Marking	White Epoxy Ink or Laser
Packing	Tray/Tubes/Tape and Reel

Reliability

Moisture Sensitivity	MSL 3, JEDEC J-STD-020
Autoclave	121°C, 15 psig, 168 Hours
Temperature Cycle	-65°/+150°C, 500/1000 Cycles
HTSL Unbiased	150°C, 1000 Hours
HAST Unbiased	130°C, 85% RH, 96 Hours
Level 2 (board level)	Available
All Reliability Tests	JEDEC Compliant

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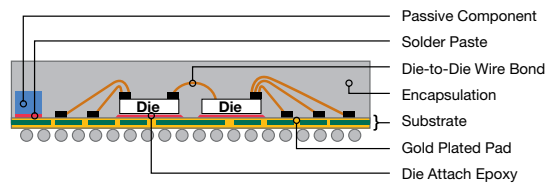
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Typical Cross Sections

Array



Leaded

