How To Meet the Demand for Smaller Packages without Sacrificing Performance

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For over five decades the semiconductor industry has relied on leaded packages as the primary solution for devices ranging in the 2 to 208-leadcount-market segments. General industry familiarity with the package and widespread acceptance among end customers kept products such as clocks, buffers, gate arrays, and drivers for hand held applications from migrating to the newer packaging technologies. In the last two years we have seen a slow transition start to occur. Changes in end market size constraints, new package technologies, and perhaps most importantly lower cost solutions are driving a migration to leadless packages.

QFP packages and its variations, the MQFP, TQFP, etc. have been a significant player in the leaded package market since being introduced in the sixties. In today's market where space is a premium and high frequency is desired, the QFP's relatively large body size and leads present significant drawbacks. In addition, the leads add complexity to the manufacturing and test process via forming steps, inspection steps and handling requirements. This drives to the requirement to move to a leadless package.

Traditional leadless packages such as fpBGAs and QFNs have been unable to gain widespread acceptance as replacements for leaded packages due to cost, pin count or performance drawbacks. In 2003, a new leadless package entered the market, the Thin Array Plastic Package. Currently offered by more than one semiconductor company, the TAPP™ offers a viable solution. The TAPP is a high-density package with superior electrical and thermal performance as compared to a QFP. As an illustration of the superior thermal performance, figure 1 shows a thermal performance comparison between a 10x10 TAPP and a 10x10 QFP. The TAPP's performance is far greater than the QFP. So when converting from larger body QFPs to smaller TAPP the inherent thermal performance characteristics of the TAPP allow for a smaller package to provide adequate if not better thermal dissipation.

Take for example the packages shown in figure 2. The product was originally packaged in standard 10x10mm 64 lead QFP. By using the TAPP technology the design was converted to a 6x6mm package. Additional benefits are reduction of overall package height by 33% and greater than 20% reduction of wire length. The leadless package reduced the overall size, met the pad requirements while exceeding the electrical and thermal performance of the QFP. By reducing the body size to a fraction of the original QFP size, the new package is lower in cost and reduces overall product cost by allowing for the use of a smaller PCB. For even larger QFPs the size reduction is much more dramatic.

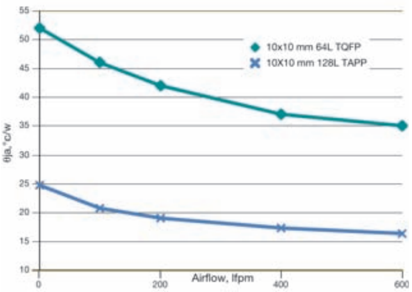


Figure 1.

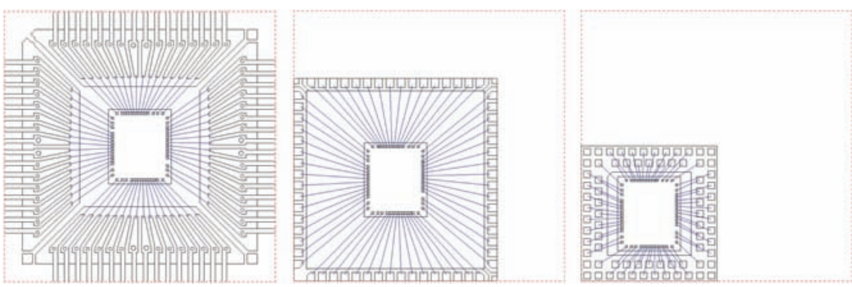
Enabling technologies in the TAPP are multiple rows of pads, which can be placed at virtually any pitch down to 0.4mm. The innovative manufacturing technology allows for a segmented "ground" ring that is electrically isolated which can be used for powers and grounds to reduce the number of peripheral pads. Direct paths for signals and heat offer excellent performance without the RLC draw backs caused by leads. Package sizes are currently available up to 19x19mm with package height as thin as .4mm.

Another consideration is the emerging market demand for lead-free packages. While a growing number of packages offer lead-free solutions, the TAPP is inherently lead-free. All options are PB free and Green to meet the emerging demand for environmentally sensitive products.

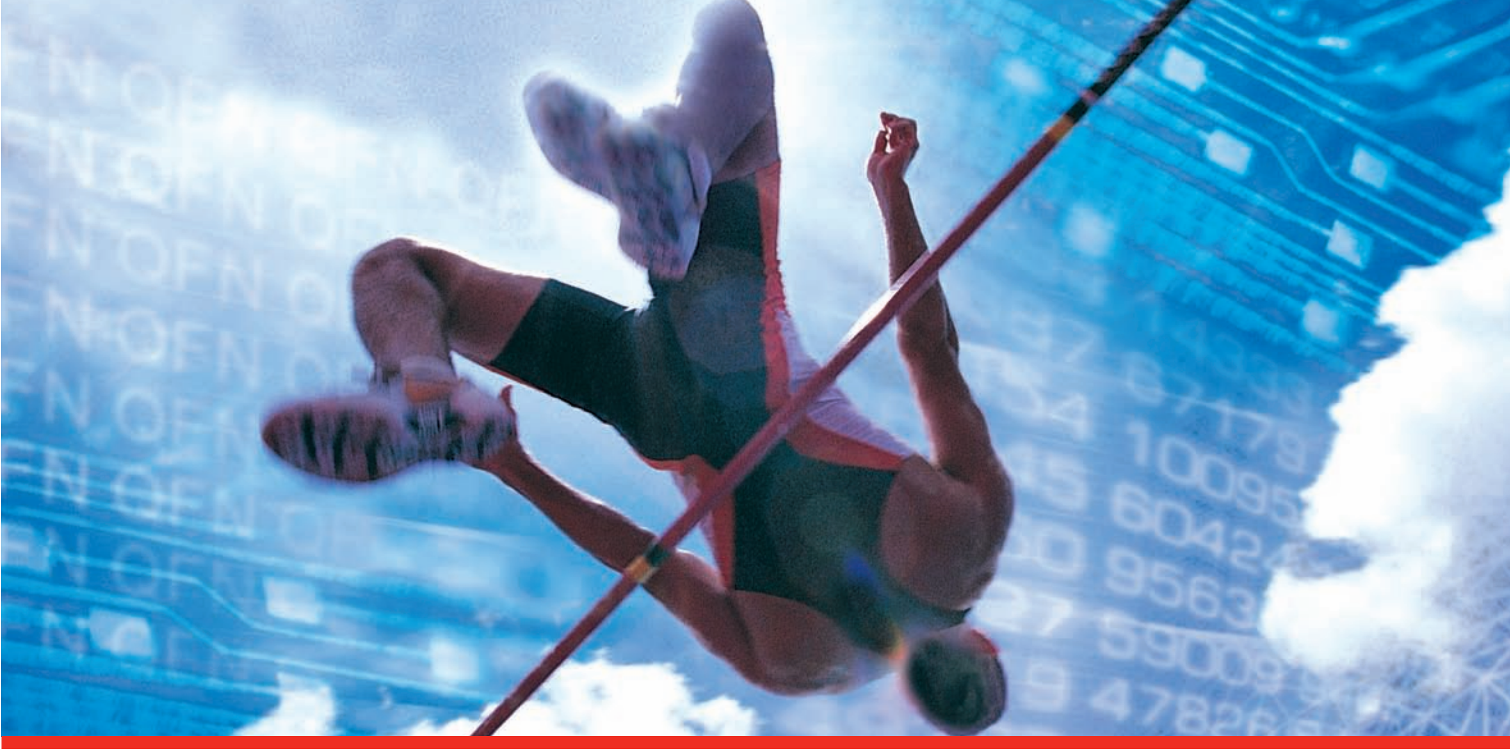
In designing a new IC, certain early considerations will allow for a TAPP like package to be used. Grouping, on the die, of powers, grounds, and signals that can be bundled at the package greatly simplifies the design of a single layer package and allows for a smaller overall package size. Die size to package size ratio considerations which meet design guidelines ensure the manufacturability of the package. Certain SATS providers have package design teams in local offices, which will work with customers to find the optimal package solution.

By no stretch of the imagination is it anticipated that leaded packages disappearing all together as not all products are good candidates for conversion. In some cases leaded packages offer a better overall solution. The focus of any packaging program should be to provide the most effective package for the application. However, as the market continues to drive for increased performance in smaller spaces, leadless packages such as the TAPP will be the replacement for traditional leaded packages that can no longer meet the market requirements. ◆

Figure 2.

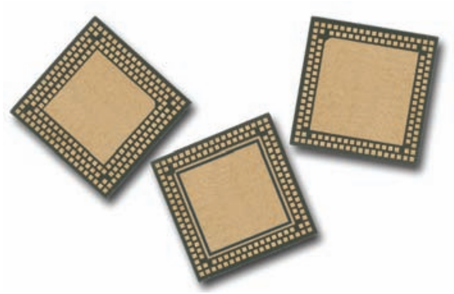


10x10 mm 64 LQFP (FP=2.0)	9x9 mm 64 QFN	6x6 mm 76 TAPP
Wire length = 91 mils	Wire length = 150 mils	Wire length = 71 mils
Over-all thickness = 1.2 mm	Over-all thickness = 1.0 mm	Over-all thickness = 0.8 mm
PCB Area = 1.0	Area = 0.56	Area = 0.25



The Best QFN Just Got Better

ASAT's Next Generation QFN: TAPP.
More I/Os, 3 Pad Rows, Smaller Form Factor.



If smaller is better, then this is the best: Announcing the next step in QFN revolution; ASAT's TAPP™ (Thin Array Plastic Package). TAPP's smaller size and thinner profile takes up less circuit board space, making it ideal for high-performance applications in today's compact devices. And more than just small, it offers enhanced thermal performance and superior electrical characteristics along with natural strip test capabilities. Plus, with its JEDEC approval, lead-free TAPP meets today's demanding industry standards.*

If anybody could make it better, it's no surprise that it's ASAT. After all, we're the company that pioneered the QFN in the first place.

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* TAPP packaging specifications have Microelectronics Outline MO-247B and Design Standard JEP95 Sec. 4.19 approval from the Joint Electron Device Engineering Council (JEDEC).